EXHIBIT J

PATENT
Attorney Docket No.: 18865-17US
Client Reference No.: 17732/722600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

29/D
6-12-01
T. Flowers

In re application of:

Sze-Ki Mo, et al.

Application No.: 08/970,221

Filed: November 17, 1997

For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE

Examiner: Jackson Jr., J.

Art Unit: 2815

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 5, 2000, please amend the above-captioned patent application as set forth below.

IN THE CLAIMS:

Please cancel claims 13, 18-22 and 54 without prejudice to renewal and amend claims 1, 8, 47, 50, 53 and 55 as set forth below. A marked-up version of the amended claims is included at the end of the remarks section.

1. (Thrice Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

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a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

68. (Thrice Amended) An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

15 47. (Twice Amended) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

D3

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

18 50. (Twice Amended) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

D4

21 53. (Once Amended) The trenched field effect transistor of claim 6, further comprising:

D5

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

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These claims were added for the specific purpose of further distinguishing over the cited reference Hshieh '543. Hshieh '543 teaches forming an N+ buried layer (16) between the epitaxial N- layer (or drift region 4B) and the substrate 10 to ensure "that avalanche breakdown occurs at the buried layer/body region ...." [Hshieh '543, col. 2, lines 6-10]. Applicants were the first to find that a trench transistor structure can be formed with a shallow heavy body structured in a way that the need for such buried layers is eliminated with very little, if any, compromise in the transistor cell density. Applicants respectfully submit that, for the reasons discussed below, there should be no ambiguity associated with the claimed structure which specifies the relative depths of the heavy body and the well regions in the trench transistor (see below). Applicants have nevertheless amended claims 50, 53 and 55 to remove the language the rejection finds vague. Withdrawal of this rejection is therefore respectfully requested.

- Section 102(e) or 103(a): Hshieh '543

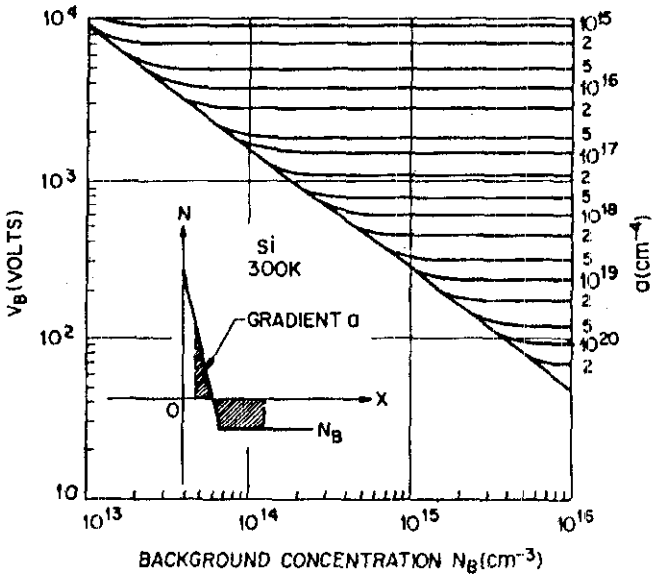
The Office Action maintains the previous rejection of claims 1, 2, 6, 8-11, 46-53, and 55 under 35 U.S.C. §102(e) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Hshieh '543. The rejection states:

> "Applicant's argument that Hshieh does not disclose an 'abrupt' junction is unpersuasive. The junction in Hshieh is abrupt. There are no particularly claimed dopant concentrations which would structurally distinguish applicant's 'abrupt' junctions over the 'abrupt' junctions of the applied art. Accordingly 'abrupt' is merely a label which does not structurally distinguish applicant's claims over the applied art."

Applicants respectfully submit that this rejection not only mischaracterizes the technical import of the claim language, it misconstrues well-established law regarding adequacy of claims. The terminology "abrupt junction" is well-known to those skilled in the art as having a very well-defined meaning with specific structural significance. "Physics of Semiconductor Devices," by S.M.Sze is considered a seminal book on the subject and is widely used throughout the academic community as well as the industry. Sze devotes an entire section (section 2.3.1) on the "Abrupt Junction," and states the following at page 72: "In

practice, most impurity profiles can be approximated by the following two limiting cases: the abrupt junction and the linearly graded junction ...." Sze also explains the "profound effects" of these differently formed junctions on the "avalanche multiplication process." [Sze, bottom of page 73]. After a detailed analysis of the characteristics of the "abrupt" junction versus the "linearly graded" junction, at page 104, Sze presents the following:

> "An approximate universal expression can be given as follows for the results above comprising all semiconductors studied: :
>
> $$V_B \cong 60(E_g/1.1)^{3/2}(N_B/10^{16})^{-3/4} \quad \text{V} \qquad (79a)$$
>
> for abrupt junctions where E_g is the room-temperature bandgap in eV, and N_B is the background doping in cm-3; and
>
> $$V_B \cong 60(E_g/1.1)^{6/5}(a/3x10^{20})^{-2/5} \quad \text{V} \qquad (79b)$$
>
> for linearly graded junctions where a is the impurity gradient in cm-4.
>
> For diffused junctions with a linear gradient on one side of the junction and a constant doping on the other side (shown in Fig. 31, insert), the breakdown voltage lies between the two limiting cases considered previously 39 (Figs. 26 and 28). For large a and low N_B, the breakdown voltage of diffused junctions (Fig. 31) is given by the abrupt junction results (bottom line); on the other hand, for small a and high N_B, V_B will be given by the linearly graded junction results (parallel lines)."



Accordingly, referring to Fig. 31 of Sze (reproduced above for convenient reference), for a given background doping N_B, the breakdown voltage V_B is lowered (parallel lines) as the impurity gradient *a* increases until it comes to a limit at the point (on the bottom line) where the impurity gradient *a* reaches an abrupt junction, after which V_B remains constant. Thus, contrary to the rejection's characterization, "abrupt" is clearly neither "merely a label" nor is it devoid of any structural significance.

Furthermore, the rejection's assertion that "there are no particularly claimed dopant concentrations which would structurally distinguish applicant's 'abrupt' junctions over the 'abrupt' junctions of the prior art" is flawed in two respects. First, no where in Hshieh '543 could there be found any mention of any junction being "abrupt." Secondly, it is well-established that mathematical precision should not be imposed on claim language for its own sake, and that an applicant has the right to claim the invention in terms that would be understood by persons of skill in the field of invention. *Modine Mfg. Co. v. United States ITC*, 75 F.3d 1545, 37 USPQ2d 1609 (Fed. Cir. 1996). This is particularly relevant in the present case where not only the structural significance of the terminology "abrupt junction" is well understood by those skilled in this art, the number of different variables involved in a structure that is an "abrupt junction" (e.g., background doping, gradient, target breakdown voltage, etc.) renders it meaningless to provide, for example, specific doping concentrations without specifying numbers for other variables. Furthermore, any numbers would also be rendered meaningless given the well-known and ever aggressive miniaturization process over time in the field of semiconductors. Dimensions such as junction depths employed in semiconductor devices at any given time often become obsolete within a two to three year period. In fact, products that are now being manufactured based on the teachings of the instant invention no longer employ the exemplary numbers provided in the instant specification (filed in November of 1997). Thus, requiring specific doping concentrations or other mathematical limitations where none should be required would unnecessarily and unfairly limit the scope of the claim applicants are otherwise entitled to.

Independent claims 1, 8 and 47 all specify the junction formed between the "heavy body" and the "well" as being "abrupt" and, for the above reasons, therefore distinguish over the cited art. These claims, however, include additional elements that further distinguish over the cited references. Claim 1, for example, also recites "the depth of the [heavy body] junction relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench ...." Again, no combination of the cited prior art teaches or suggests the claimed structure. In maintaining its rejection of the claim, however, the Office Action states: " Arguments regarding 'controlled' are unconvincing of patentability because the claimed structure does not functionally or structurally distinguish over the applied art." It is difficult to follow the reasoning behind this rejection since the relevant claim language, on its face, does clearly distinguish in both those respects. Structurally, the relevant claim language defines a specific depth for the "heavy body," and functionally, it specifies the moving away or spacing away of the "transistor breakdown initiation point ... from the trench." Contrary to the rejection's assertion, this combination clearly distinguishes over the cited references. With respect to the depth of the P+ region 24 in Hshieh '543, a reading of Hshieh '543 makes it clear that the inventors had no clue whatsoever about the possibility of having a P+ region (24) that is shallower than the well (18) and yet is capable of addressing the breakdown problem by its structure (i.e., depth and abruptness of its junction). This is so because Hshieh '543 clearly shows a P+ region 24 that is as deep or deeper than the well 18 in every figure, and in the only instance where they make a cursory mention of shallower "P+ body contact regions 24", they immediately add "... in which case the breakdown current conduction path is from body region 18 to buried layer 16." [Hshieh '543, col. 3, lines 1-6]. Hshieh '543 therefore teaches nothing more than what was already known in the art; that if the P+ body region 24 is made shallower than the well, the device would then need some other additional structure to control the point of breakdown initiation (see further discussion below). This additional structure, as taught by Hshieh '543, is an N+ buried layer 16. Hshieh '543 therefore clearly fails to teach or suggest a heavy body that is shallower than the well, and has its depth "relative to the depth of the well, [] adjusted so that a transistor breakdown initiation point is spaced away from the trench ...."

Although not clear, in light of the §112, 2nd ¶ rejection above, it is assumed that the Examiner may have had difficulty with the use of the word "controlled." While it is not deemed necessary, to the extent that the Examiner may consider "adjusted" more appropriate in defining a structure, Applicants have amended independent claims 1, 8 and 47 to replace the word "controlled" with "adjusted." Applicants are entitled to claim this structural aspect of the present invention (i.e., relative depths of the heavy body and the well), that is also further defined functionally (impacting breakdown initiation point), without having to limit the claim to specific numerical dimensions. Applicants welcome Examiner's suggestions for any substitute words for "controlled" or "adjusted."

Hshieh '543 thus clearly neither teaches a trench field effect transistor with a "heavy body" that forms an "abrupt junction" with the well, nor one that has a "heavy body" with a depth relative to the depth of the well that causes "a transistor breakdown initiation point [to move] away from the trench." Nor does Hshieh '543 even remotely suggest the claimed combination. In fact, by teaching that a buried layer (16) is required to address the breakdown problem, Hshieh '543 teaches away from a structure that can accomplish similar functionality with a clever expedient as that of the claimed "heavy body." To be sure, the notion that a prior art diagram may "look similar" to a diagram that depicts an aspect of the invention, cannot be the basis for a 102 or 103 rejection. Often times diagrams are not to scale and significant novel and non-obvious structural features such as depth or abruptness of a junction in semiconductor technology may not be easily depicted. Again, both the diagrams and the body of Hshieh '543 not only fail to teach but also fail to suggest the claimed invention.

Independent claims 1, 8 and 47 are thus patentably distinguished over Hshieh '543. Claims 2, 5-7, 9-12, 14-17, 46, 48-53 and 55 depend from one the claims 1, 8 and 47 and therefore derive patentability therefrom. These claims, however, recite additional novel and non-obvious features that further distinguish over Hshieh '543. Claims 48 and 49, for example, describe an alternating source and heavy body contact arrangement along the longitudinal axis of a trench. No such structure is taught or suggested by Hshieh '543. Claims

50, 53 and 54, for example, specifically recite a heavy body which has its depth relative to the depth of the well "adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate." Hshieh '543 teaches the opposite: forming a "buried layer" (16) between the epitaxial layer (or drift region) and the substrate. Claims 1-2, 5-12, 14-17, 46-53 and 55 are therefore patentably distinguished over Hshieh '543. Accordingly, withdrawal of this rejection is respectfully requested.

- Section 103(a): Hshieh '543, Darwish '725, Nakamura '491, Bencuya '324, and Harada '050

Claims 1, 2, 5-12, 14-22, 46-55 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hshieh '543 with Darwish '725, applicant's prior art admissions, Nakamura '491, Bencuya '324, and Harada '050. The rejection does not provide an explanation of any new grounds of rejection other than to state: "Harada additionally teaches a termination structure including a deep well connected to body regions. It would have been obvious to have practiced the same with Hshieh to have improved breakdown voltage. The previous rejection with the above comments applies."

With respect to claims 1, 8 and 47, and all claims depending therefrom, as discussed above, Hshieh '543 clearly fails to teach or suggest the invention as claimed. None of the other cited references, or any combination thereof, including any admitted prior art, adds anything that would support a finding of unpatentability. If anything, a close look at every one of these references, as well as many of the other relevant prior art of record, provides overwhelming evidence of non-obviousness of the claimed invention. This is so because these prior art references, one after another, demonstrate the fact that many of the most skilled artisans in the field recognized and struggled with the exact same set of challenges (e.g., increased trench MOSFET cell density, improved breakdown voltage, lowered transistor on-resistance, etc.), yet none were able to conceive of the solution claimed by the present invention. Instead, in each instance, the prior art proposes a solution that is fundamentally different both structurally and functionally, as well as being technically inferior as demonstrated by the commercial success of the products manufactured based on the present invention. To stress this point, Applicants present below a brief analysis of a number of the

cited prior art references. A declaration evidencing the commercial success as another objective measure of non-obviousness is separately submitted.

- **Hshieh '543**

An analysis of this reference has already been presented, however, since it forms the main basis for rejection of the claims, it is repeated here in a more concise fashion.

Recognition of the Problem:

"However it is also known that when cell density is high as in the typical trenched transistor structure, a new undesirable JFET phenomenon gradually appears between the P+ deep body regions 5. The P+ deep body regions 5 typically extend from a principal surface of the semiconductor material into the P body region 7 to provide a contact to the P body region 7. These deep body regions 5 ensure that avalanche breakdown occurs in these regions rather than at the bottom of the trenches. This undesirable JFET phenomenon is because such deep body regions 5 are relatively close to each other. (Also shown in FIG. 1 are conventional drain electrode 8B and source-body electrode 8A.) Thus while avalanche breakdown occurs rather than destructive breakdown at the trench bottom, i.e. breakdown damaging the insulating oxide at the trench bottom, undesirably this new JFET resistance makes a bigger contribution to drain-source on resistance when cell density is higher." [Col. 1, lines 29-49, emphasis added].

Proposed Solution (Figs. 2 & 3F):

"Further, in accordance with the invention a doped buried layer [16]is formed in the upper portion of the drain region [10] and in contact with the drift region [14]. This buried layer has the same doping type as that of the drain region and a doping concentration higher than that of the drift region, and is typically located to directly underlie the body contact (deep body) region formed between each pair of adjacent source regions. The buried layer is heavily doped to form N+ doped fingers extending into the drift region. This buried layer [16] is typically formed prior to the epitaxial growth of the drift region, and by having an optimized doping profile ensures that avalanche breakdown occurs at the buried layer/body region or buried layer/body contact region. Hence the distance between the lower part of the body contact or body region and the upper part of the buried layer determines breakdown." [Col. 1, line 65 to col. 2, line 13, reference numerals and underlining added].

- **Darwish '725**

Recognition of the Problem:

"The deep central P+ region 114 in MOSFET 300, while greatly reducing the adverse consequences of breakdown, also has some unfavorable effects. First, an upward limit on cell density is created, because with increasing cell density P ions may be introduced into the channel region. As described above, this tends to increase the threshold voltage of the MOSFET. Second, the presence of a deep P+ region 114 tends to pinch the electron current as it leaves the channel and enters the drift region 111. In an embodiment which does not include a deep P+ region (as shown in, for example, FIG. 2A), the electron current spreads out when it reaches the drift region 111. This current spreading reduces the average current per unit area in the drift region 111 and therefore reduces the on-resistance of the MOSFET. The presence of a deep central P+ region limits this current spreading and increases the on-resistance consistent with high cell densities. What is needed, therefore, is a MOSFET which combines the breakdown advantages of a deep central P+ region with a low on-resistance." [Col. 3, lines 28-48, emphasis added].

Proposed Solution (Figs 4 & 5):

"When the MOSFET is turned on, an electron current flows vertically through a channel within the body region adjacent the trench. To promote current spreading at the lower (drain) end of the channel region when the MOSFET is turned on, a "delta layer" [402] is provided within the drift region. The delta layer is a layer wherein the concentration of dopant of first conductivity type is greater than the concentration of dopant of first conductivity type in the drift region generally. In many embodiments the delta layer abuts the body region, although in some embodiments the delta layer is separated from the body region. The upper boundary of the delta layer is at a level which is above the bottom of the trench in which the gate is formed. In some embodiments, the upper boundary of the delta layer coincides with a lower junction of the body region. The lower boundary of the delta layer may be at a level either above or below the bottom of the trench." [Col. 3, lines 64 to col. 4, line 13, reference numeral and underlining added].

- **Hshieh '128** (Office Action mailed 8/4/99)

Recognition of the Problem:

"In typical DMOS transistors using a trenched gate electrode, in order to avoid destructive breakdown occurring at the bottom of the trench into

the underlying drain region, such transistors are fabricated so that a P+ deep body region extends deeper than does the bottom of the trench into the substrate (drain region). Thus rather than destructive breakdown occurring at the trench bottom, instead avalanche breakdown occurs from the lowest portion of this P+ deep body region into the underlying drain region. However due to device physics limitations, the cell density of such transistors is thereby restricted by lateral diffusion of this P+ deep body region. That is, in order to provide a P+ deep body region that extends deep enough into the substrate, the drive in step causes this P+ deep body region to diffuse laterally. If it diffuses too far laterally, it may coalesce with an adjacent P+deep body region and degrade transistor performance.

Hence, in order to allow deep enough extension of the P+deep body region into the substrate, the transistor cells each must be relatively large in surface area so that the lateral diffusion does not allow such coalescing. This increases the surface area consumed by each cell, or in other words increases the size of the transistor. As is well known, it is a primary goal of power MOSFET fabrication to minimize chip surface area. This lateral diffusion of the P+deep body region prevents optimization of transistor density and hence wastes chip surface area." [Col. 1, lines 25-51, emphasis added].

Proposed Solution (Figs. 1, 2 & 3):

In accordance with the invention, cell density is increased in a DMOS transistor. In some embodiments this is accomplished by providing a very narrow (in lateral dimension) P+deep body region [16 in Fig. 1] with little or no lateral diffusion. ... In a second embodiment, in addition to the high energy P+deep body implant [36 in Fig. 2], a double epitaxial layer [12 and 34 in Fig. 2]is provided underlying the body region [14], with the P+deep body P+region [34] not extending below the depth of the trench. Instead, the double epitaxial layer provides the desired current path away from the bottom of the trenches. ... In a third embodiment, there is no P+deep body implantation at all and instead only the double epitaxial layer [12 & 34 in Fig. 3] is used underneath the body region." [Col. 1, lines 54 to col. 2, line 19, reference numerals and underlining added].

Two more examples of prior art references evidencing the fact that designers attempting to solve the same problem have failed to arrive at a solution that is even remotely suggestive of the present invention are provided below. An earlier issued patent (USPN 5,072,266) illustrates the fact that the specific challenges have been known for well over a

decade, and a second more recently issued patent (USPN 5,998,836) shows a contemporaneous attempt at solving the problem. Both offer solutions that are widely different than that proposed and claimed by the present invention.

- **5,072,266 (Bulucea et al.)**

Recognition of the Problem:

"An engineering trade-off must be made between on-resistance, breakdown voltage and other engineering figures of merit so that the perimeter-to-area ratio Z/A advantage of the open-cell is lost. Given these constraints, the closed-cell geometry appears to be more practical. However, the closed cell geometry has at least three associated problems that do no appear to have been reported on in the technical or patent literature. The first problem is semiconductor surface breakdown. ... This junction is thus exposed to electric field line crowding and to breakdown in the epitaxial material adjacent to the bottom corners of the trench, when the device is biased in the BVDSS condition." [Col. 4, lines 24-41, emphasis added].

Proposed Solution (Fig. 8):

"This invention provides an optimized version of a power metal-oxide-semiconductor field-effect transistor (MOSFET) [wherein bulk] breakdown voltage is achieved by using a two-dimensional, field shaping, dopant profile that includes a central deep p+ (or n+) layer [27c] that is laterally adjacent to a p body layer ...." [Col. 1, lines 50-61, reference numeral and emphasis added].

"FIG. 8 illustrates one embodiment of the invention, showing half of a hexagonally shaped trench DMOS structure 21. The structure includes ... a body region 27 [where] a central portion 27c of the body region lies below a plane that is defined by the bottom of the trench 29 for the transistor cell." [Col. 6, lines 28-60]

- **5,998,836 (Williams)**

Recognition of the Problem:

"Two critical characteristics of a power MOSFET are its breakdown voltage, i.e., the voltage at which it begins to conduct current when in an off condition, and its on-resistance i.e., its resistance to current flow

when in an on condition. The on-resistance of a MOSFET generally varies directly with its cell density, since when there are more cells per unit area there is also a greater total "gate width" (around the perimeter of each cell) for the current to pass through. The breakdown voltage of a MOSFET depends primarily on the doping concentrations and locations of the source, body and drain regions in each MOSFET cell." [Col. 1, lines 32-44, emphasis added].

Proposed Solution (Fig. 3):

"In accordance with this invention, there is created in the chip a protective diffusion of the second conductivity type [38], which forms a PN junction [39] with first conductivity material in the epitaxial layer [14] or substrate. This PN junction functions as a diode. A metal layer [36] ties the protective diffusion (i.e., one terminal of the diode) to the source regions [34] of the MOSFET cells such that the diode is connected in parallel with the channels of the MOSFET cells." [Col. 2, lines 60 to 68, reference numerals and underlining added].

The above analysis holds true for many of the other prior art references of record. This demonstrates that for well over a decade engineers in the field have attempted to arrive at a design for a trench MOSFET that addresses breakdown voltage, on-resistance and cell density in an optimized fashion. It also demonstrates that time and again a solution is proposed that is very different than that found by the Applicants. If the present invention as claimed were obvious, as the rejection contends, one would have to ask why then did no person of skill in the art arrive at this solution years ago. One answer to this question may be the fact that there has been a general understanding by those skilled in this art that, in terms of impact on the electric field, between the deeper well (or body) region and a heavily doped body region that is shallower than the well, the deeper well region (that is closest to the epitaxial layer) dominates. This had led to a generally accepted assumption that such shallow heavy body junction inside a graded body junction, no matter how deep, could not have any measurable impact on breakdown voltage.

Challenging these and other accepted assumptions, and through exhaustive experimentation and computer simulations, Applicants were the first to find that the problem can in fact be addressed optimally by employing, in combination with the other features of the

transistor, a shallow heavy body with specific depth and junction characteristics. The solution offered by the instant invention requires no additional structures as proposed by numerous prior art references such as buried layers or dual epitaxial layers, delta layers, protective PN junction diodes, deep P+ body regions, etc. A family of trench MOSFET products embodying the Applicants' elegant solution, which has clearly not been taught or suggested by the art of record, has enjoyed tremendous commercial success as a direct result of the benefits of the claimed invention. To provide further objective evidence of non-obviousness of the claimed invention, Applicants herewith submit a declaration by the Senior Vice President of Discrete Power Products of the Assignee demonstrating this commercial success.

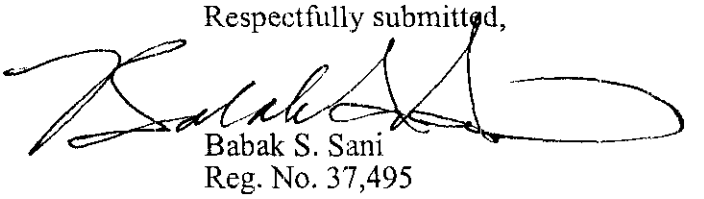
Accordingly, none of the cited references, or any combination thereof, teach or suggest a trench transistor having a "heavy body" that forms an "abrupt junction" inside a well, and whose depth is adjusted to impact the location of breakdown initiation. Every independent claim pending in the instant application recites this combination. All pending claims are therefore patentably distinguished over the art or record. Withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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Marked-Up Version of Amended Claims – Appln. No. 08/970,221

2. (Thrice Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is **[controlled]** adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

8. (Thrice Amended) An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well **[junction]**, and a depth of the heavy body relative to a depth of the well**[,]** is **[controlled]** adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

47. (Twice Amended) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction**[,]** relative to a maximum depth of the well, is **[controlled]** adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

50. (Twice Amended) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate

[wherein the the relative depths of the doped heavy body and the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate].

53. (Once Amended) The trenched field effect transistor of claim 8, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate

[wherein the relative depths of the deepest portion of the heavy body and a depth of the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate].

55. (Once Amended) The trenched field effect transistor of claim 47, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to **[and]** a depth of the well **[are controlled]** is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

GP-1107 2615

PTO/SB/21 (08-00)

Please type a plus sign (+) inside this box → [+]

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	08/970,221
Filing Date	November 17, 2000
First Named Inventor	Brian Sze-Ki Mo, et al.
Group Art Unit	1107
Examiner Name	Jerome Jackson, Jr.
Total Number of Pages in This Submission: 35*	Attorney Docket Number: 018865-001700US

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment / Response
  - [ ] After Final
  - [x] Affidavits/declaration(s)
- [x] Extension of Time Request
- [ ] Express Abandonment Request
- [x] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition Routing Slip (PTO/SB/69) and Accompanying Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below)*:

***A page count of the references and publications is not included..**

Remarks: The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Babak S. Sani — Reg No. 37,495
Signature	
Date	June 4, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: June 4, 2001

Typed or printed name	Deborah Bullock		
Signature		Date	June 4, 2001

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SF 1229985 v1

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1070

Complete if Known	
Application Number	08/970,221
Filing Date	November 17, 1997
First Named Inventor	Sze-Ki Mo, Brian
Examiner Name	Jerome Jackson, Jr.
Group Art Unit	1107
Attorney Docket No.	18865001700

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1430

Deposit Account Name: Townsend and Townsend and Crew LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ **Payment Enclosed:**

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20**	=	X		=	
Independent Claims		-3**	=	X		=	
Multiple Dependent				X		=	

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Large Entity Fee ($)	Small Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	890
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of Information Disclosure Stmt	180.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

The Commissioner is authorized to charge any additional fees to the above noted Deposit Account.

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)180

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Babak S. Sani	Registration No. (Attorney/Agent)	37,495	Telephone	415-576-0200
Signature				Date	June 4, 2001

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